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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PATEL, DHARTI HARIDAS	

ART UNIT	PAPER NUMBER
2836	

NOTIFICATION DATE	DELIVERY MODE
03/12/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/588,984	DEUTSCHMANN ET AL.	
	Examiner	Art Unit	
	DHARTI H. PATEL	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/10/06, 12/11/06, 11/01/07, 10/27/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 4, 9 and 15 are objected to for the following informalities.

Claims 4, 9 and 14 depend on claim 21. Claims cannot refer to a preceding claim.

MPEP 608.01. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 6-12, 15, 17-19 and 21are rejected under 35 U.S.C. 102(b) as being unpatentable over Lin, Patent No. 5,982,601.

With respect to claim 1, Lin discloses a circuit arrangement for protecting an integrated semiconductor circuit comprising: a protection circuit [Fig. 6B; consists of SCR transistors], which contains a thyristor structure [Fig. 6B; SCR] and is connected located between an element to be protected [Fig. 6B; load connected to VDD bus] and a reference potential [Fig. 6B; GND], the protection circuit comprising a thyristor structure that includes active elements [Fig. 6b; SCR includes active elements such as bipolar transistors]; and a control circuit [Fig. 6B; consists of capacitor C2 and resistor R2] configured to drive for driving the protection circuit [Fig. 6B; SCR] by generating a plurality of control signals to drive one or more active elements of the protection circuit [Fig. 6B; signals coming out from RC to inverters to gates of bipolar transistors].

With respect to claim 2, Lin discloses that the control circuit comprises a detector circuit [Fig. 6B; C2 and R2], which, on the input side, is connected in parallel with the protection circuit [Fig. 6B; RC and SCR are connected in parallel].

With respect to claim 3, Lin discloses that the detector circuit comprises a first resistive-capacitive (RC) element, the first RC element (R1, C1) comprising a resistor [Fig. 6B; R2] and a capacitor [Fig. 6B; C2].

With respect to claim 4, Lin discloses that the switching elements comprise inverters [Fig. 6B; inverters X1-X4].

With respect to claim 6, Lin discloses that the detector circuit [Fig. 6B; resistor R2 and capacitor C2] of the control circuit is configured to identify a signal with a predetermined rise time at the element to be protected [Fig. 6B; PAD; col. 4 lines 8-21].

With respect to claim 7, Lin discloses that the control circuit comprises a plurality of time- dependent elements [Fig. 6B; resistor R2 and capacitor C2] which configured to determine a duration of activation of the control circuit [col. 4 lines 8-21].

With respect to claim 8, Lin discloses that the time-dependent elements comprise resistive-capacitive (RC) elements [Fig. 6B; resistor R2 and capacitor C2; col. 4 lines 8-21].

With respect to claim 9, Lin discloses that the detector circuit [Fig. 6B; transistor M2] and the switching elements each comprise individual transistors [Fig. 6B; each inverter X1-X4 consists of pair of transistors].

With respect to claim 10, Lin discloses that detector circuit [Fig. 6B; RC elements] is configured to identify a signal with a predetermined rise time at the element

[Fig. 6B; pad] to be protected, the predetermined rise time being a detection criterion of the detector circuit [col. 4 lines 8-21].

With respect to claim 11, Lin discloses that the control circuit comprises at least some time-dependent elements [Fig. 6B; RC elements R2 and C2] configured to determine a duration of the control circuit [col. 4 lines 8-21].

With respect to claim 12, Lin discloses that the detector circuit comprises at least one resistive-capacitive [RC) element [Fig. 6; RC elements R2 and C2], the at least one RC element comprising a resistor [Fig. 6B; R2] and a capacitor [Fig. 6B, C2].

With respect to claim 15, Line discloses that the switching elements comprise individual metal oxide semiconductor (MOS) transistors [Fig. 6B; inverters X1-X4 comprises a pair of MOS transistors].

With respect to claim 17, Lin discloses that control inputs of the active elements of the protection circuit in comprise a semiconductor structure [Fig. 7, Fig. 8] that includes wells of different conductivity types, the wells including highly doped regions for output circuits of the active elements [Fig. 6B; bipolar transistors of SCR].

With respect to claim 18, Lin discloses a method for protecting an integrated semiconductor circuit, the method comprising: detecting a state of an element [Fig. 6B; PAD] to be protected using a protection circuit [Fig. 6B; SCR] located connected between the element to be protected and a reference potential [Fig. 6B; GND], the protection circuit comprising a thyristor structure [Fig. 6B; SCR structure consisting two bipolar transistors] that includes active elements [Fig. 6B; bipolar transistors]; using a control circuit [Fig. 6B; RC elements R2 and C2] to generate a plurality of control signals

based on a detected state of the element to be protected [col. 4 lines 8-21]; and communicating the control signals to a control input of the active elements of the protection circuit [Fig. 6B: communicating the signals to the gates of transistors of SCR via inverters X1-X4].

With respect to claim 19, Lin discloses that the RC elements are configured to generate control signals for controlling a begging of activation [Fig. 6B; during an ESD event] and an end of activation [Fig. 6B; under normal operation] of the control circuit.

With respect to claim 21, Lin discloses that upon detection of a detection criterion, the control circuit [Fig. 6B; RC elements] is configured to drive switching elements [Fig. 6B; transistors of inverters X1-X4] that are configured to generate the control signals [Fig. 6B; signals coming out from inverters X1-X4].

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Mergens et al., Patent No. 6,803,633.

With respect to claim 1, Mergens discloses a circuit arrangement for protecting an integrated semiconductor circuit comprising: a protection circuit [Fig. 7; consists of

116 and 118 SCR transistors], which contains a thyristor structure [Fig. 7; SCR] and is connected located between an element to be protected [Fig. 7; 104] and a reference potential [Fig. 7; 112], the protection circuit comprising a thyristor structure that includes active elements [Fig. 7; SCR includes active elements such as bipolar transistors 116 and 118]; and a control circuit [Fig. 7; 706] configured to drive for driving the protection circuit [Fig. 7; SCR] by generating a plurality of control signals to drive one or more active elements of the protection circuit [Fig. 6B; signals coming out from control circuit 706 to inverters to gates of bipolar transistors].

With respect to claims 2 and 3, Mergens discloses that the control circuit [Fig. 6; control circuit 608] comprises a detector circuit [Fig. 6; consists of resistor 620 and capacitor CLU] in parallel with the protection circuit [Fig. 6; SCR].

With respect to claim 5, Mergens discloses that the active elements comprise active elements of differential conductivity types [Fig. 7; PNP and NPN bipolar transistors] and the plurality of control signals comprise a plurality of control signals [Fig. 7; signals coming out from T1, 108-2 and T2, 108-1] for the active elements of different conductivity types, the control signals having opposite polarities that are based on conductivity types of active elements, the control signals being configured to drive control inputs of the active elements.

With respect to claim 16, Mergens further comprises switching elements [Fig. 7; inverters 630 and 704] and driver elements [Fig. 7; PLU and NLU], the switching elements being electrically connected to the driver elements [Fig. 7; inverters 704 and 630 are connected to NLU and PLU transistors].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mergens, Patent No. 6,803,633, in view of Ker et al., Patent No. 6,465,848.

With respect to claim 13, Mergens further comprises switching elements [Fig. 7; inverters consists of MOSFETs 630 and 704]; driver elements [Fig. 7; transistor PLU and NLU] connected to the switching elements, but does not disclose a second resistive-capacitive (RC) circuit.

Ker discloses an electrostatic discharge protection circuit, which comprises a first RC circuit [Fig. 6b; 84] and a second RC circuit [Fig. 6b; 86].

Mergens and Ker are analogous electrostatic discharge protection circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Ker's second RC circuit, into Mergens, for the benefit of controlling the second gate of the SCR independent of the first gate of the SCR.

With respect to claim 14, Ker discloses that the detector circuit comprises two detector sub-circuits [Fig. 6b; 84 and 86], each of the detector sub-circuits configured to drive a switching element for the active elements of the protection circuit.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, Patent No. 5,982,601.

With respect to claim 20, Lin discloses that the switching elements each comprise MOSFETS, but does not disclose that the switching elements each comprise individual bipolar transistors. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize bipolar transistors instead of MOSFETs, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the MOSFETs with bipolar transistors, for the benefit of having bipolar transistors having higher efficiency at operating temperature, cooler running at high current densities, and higher continuous currents per the area.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DHARTI H. PATEL whose telephone number is (571)272-8659. The examiner can normally be reached on 7:00 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dharti H Patel/
Examiner, Art Unit 2836
03/04/2009

/Albert W Paladini/

Primary Examiner, Art Unit 2836 3/6/09